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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Lin, *et al.*	Docket No.:	TSM03-0670
Serial No.:	10/729,092	Art Unit:	2811
Filed:	December 5, 2003	Examiner:	TBD
For:	Structure and Method of Forming Integrated Circuits Utilizing Strained Channel Transistors		

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Respectfully submitted,

KHayes

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INFORMATION DISCLOSURE STATEMENT

The Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08A & 08B that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(b)(3), before the mailing of a first Office action on the merits.

Pursuant to 37 CFR 1.98(a)(2)(i), as amended, copies of U.S. Patents cited are not being submitted. However, Applicant has included copies of any non-patent literature.

Respectfully submitted,

5/21/04
Date

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 5

Complete if Known	
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First Named Inventor	Lin, *et al.*
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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number - Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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	23	WO 03/017336 A2	02-27-2003	Amberwave Systems Corporation		

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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
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	66	CAVASSILAS, N., *et al.*, "Capacitance-Voltage Characteristics of Metal-Oxide-Strained Semiconductor Si/SiGe Heterostructures," Nanotech 2002, Vol. 1, pp. 600-603.	
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